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The unification of space qualified integrated circuits by example of international space project GAMMA-400

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Abstract

The problem of electronic component unification at the different levels (circuits, interfaces, hardware and software) used in space industry is considered. The task of computer systems for space purposes developing is discussed by example of scientific data acquisition system for space project GAMMA-400. The basic characteristics of high reliable and fault tolerant chips developed by SRISA RAS for space applicable computational systems are given. To reduce power consumption and enhance data reliability, embedded system interconnect made hierarchical: upper level is Serial RapidIO 1x or 4x with rate transfer 1.25 Gbaud; next level - SpaceWire with rate transfer up to 400 Mbaud and lower level - MIL-STD-1553B and RS232/RS485. The Ethernet 10/100 is technology interface and provided connection with the previously released modules too. Systems interconnection allows creating different redundancy systems. Designers can develop heterogeneous systems that employ the peer-to-peer networking performance of Serial RapidIO using multiprocessor clusters interconnected by SpaceWire.

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1. Introduction

The application of microelectronic products in space conditions imposes a number of special requirements such

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as endurance ≥ 200000 hours, total ionizing dose (TID_{Si}) tolerance ≥ 200 krad, resistance to single events effects (SEE) (single event burnout (SEB), single event latch-up (SEL) and single event upset (SEU)) at linear energy transfer LET ≥ 100 MeV·cm²/mg, hardness to neutrons fluence up to 10^{13} neutrons/cm². Examples of integrated circuits of such category are specialized microprocessors of Aeroflex Inc. (66 MHz, 0.25 mkm technology, $\sim 5 \cdot 10^6$ transistors) and Atmel Co. (100 MHz, 0.18 mkm technology, $\sim 8 \cdot 10^6$ transistors) both characterizing by TID_{Si} tolerance ≥ 300 krad and SEL resistance at LET ≥ 100 MeV·cm²/mg. These microprocessors resistance to SEE is provided by special functional elements scheme solutions and error-free computational process by majorization procedure. In the near future these firms will produce new generation of such microprocessors with working frequency of 150-200 MHz and transistors amount more than 10^7 .

The additional requirement is wide operational temperature range depending on the apparatus location. This time four main standard temperature ranges for electronics exist: commercial (0 ÷ +70°C), industrial (-40 ÷ +85°C), aviation (-40 ÷ +125°C), military and space (-55(-60 for Russia) ÷ +125°C). In special cases – for example units for rocket engines control the high-temperature region (-60 ÷ +200°C) are required.

In up-to date equipment the set of distributed microcontrollers are used instead of central computer. It allows appreciably reduce number and length of interconnections, total apparatus weight and noticeably increase reliability of system as a whole. Thus, in such systems the unification of radiation and SEE hardened high-temperature integrated circuits is significant factor for cost and design time reducing.

2. The unification of elemental base, interfaces, hardware and software levels

The development of elemental base for space applications is one of the main areas of scientific activity of SRISA RAS for more than 10 last years. Uniform processor cores KOMDIV-32 and KOMDIV-64 based on MIPS-architecture were developed for both the conventional high-performance systems and space applicable systems [1-3]. The unification was achieved on modules level too [4].

Following interfaces as a basic set for space applications have been picked out:

- SpaceWire for high reliability multiprocessor computing systems of mean level performance;
- Serial RapidIO for high reliability multiprocessor computing systems of high level performance;
- Ethernet 10/100 Mbit/sec for auxiliary data transfer and backward compatibility with commercially available systems;
- MIL-STD-1553B for high reliability low-speed information interchange;
- RS232/RS485 for low-speed information interchange especially with commercially available systems;
- PCI (various physical level realization) for information interchange and extension of modules functionality;
- JTAG for equipment testing and check-out;
- SPI to control the low-speed equipment;
- Pulse commands in the form of either voltage pulse with duration $\sim 0.1 \div 0.3$ sec with amplitude equals for satellite power or “dry contacts” – switch on/switch off.

On hardware level, we suppose to implement two standard types: VPX (EUROMECHANICS standard, 6U form factor) for high-level performance systems and PCI/104-Express for compact systems.

As operating system, real-time OS (RTOS) Baget 3.0 [5, 6] was chosen. During the time of its existence, this RTOS (Baget 3.0 and its earlier version Baget 2.0) is widely used by Russian developers. More than 100 organizations over the country have used them and the system has established a reputation in designing embedded control systems. RTOS Baget 3.0 is developed based on the following general approaches:

- use of standards (ARINC 653 and POSIX 1003.1 for programming interface; C standard for C language and libraries);
- portability;
- advanced facilities for tracing, logging, diagnostics. and error handling (health monitor);
- flexible scheduling;
- object-oriented approach:

- scalability (configuration tools);
- instrumental software for developing and debugging user cross-applications;
- great number of environmental packages for creating graphics applications, databases, and mapping systems.

For the best portability, OS is divided on three main parts: main part independent on hardware, written on C language (the biggest); the second part, dependent only on central processor type, written on C or Assembler language (much smaller); modules support part containing modules drivers.

During software design, cross-development technology is used whereby, using the host computer with a general-purpose OS, the source codes and OS libraries are stored as well as the compilation and build of the boot image that is executed on the target computer under the control of RTOS are performed. For debugging in terms of the source code, a remote debugger is used.

3. The characteristics of basic integrated circuits for GAMMA-400 scientific complex

The chips outlined are intended for design of various onboard space systems with increased radiation hardness and fault tolerance induced by cosmic rays. For SEE protection are used following arrangements: additional parity bits for cache and MIL-STD-1553B memory; DICE-cells in register files with Hamming code protection hardware scrubbing; SECCDED for external memory; hardware possibility of using SRAM in TMR mode; embedded cache memory control (Memory Build-In-Self-Test MBIST); spatial separation of neighboring bits (protection from MBU); “guaranteed boot” from three parallel ROM; noiseless coding at the access to buffers memory; routing tables redundancy; special topological and schematic solutions. The distinctive features of chips outlined are presented in Table 1.

Table 1. The distinctive features of basic integrated circuits developed at SRISA RAS implementing in GAMMA-400 scientific complex.

Parameter	1907VM038	1907VM056	1907KX018
Clock rate	100 MHz	100 MHz	100 MHz
Serial RapidIO performance	2 channels 1x 4x 1.25 Gbit/sec	-	6 channels 1x 4x 1.25 Gbit/sec
SpaceWire performance	4 channels 400 Mbit/sec	8 channels 400 Mbit/sec	-
SEL LET _{th}	80 MeV·cm ² /mg	80 MeV·cm ² /mg	80 MeV·cm ² /mg
SEE LET _{th}	6 MeV·cm ² /mg	6 MeV·cm ² /mg	6 MeV·cm ² /mg
σ _{sat}	< 3·10 ⁻⁸ cm ² /bit	< 3·10 ⁻⁸ cm ² /bit	< 3·10 ⁻⁸ cm ² /bit
TID _{Si}	≥ 500 krad	≥ 500 krad	≥ 500 krad
Operating temperature	-60 ÷ +125°C	-60 ÷ +125°C	-60 ÷ +125°C
Power consumption	≤ 8 W	≤ 5 W	≤ 6 W
Package	DBGA 675	CQFP 256	DBGA 399

3.1. Microprocessor 1907VM038

System-on-chip (SOC) 1907VM038 is a 128-bit microprocessor with fast internal input-output channels. This chip is based on 0.25 mkm silicon-on-insulator (SOI) technology and SIMD (Single Instruction Multiple Data) architecture. System-on-chip 1907VM038 consists of: 32-bit RISC core processor compatible with KOMDIV architecture; 128-bit math coprocessor (CP2, > 2 Gflops), including arithmetic-logical unit (ALU), static RAM and register file; DDR2 RAM controller (access rate > 2 Gbit/sec); high-performance two-channel Serial RapidIO 1x or 4x controller (SRIO); high-performance (up to 400 Mbit/sec) four-channel SpaceWire controller (SW); 32 kByte on-chip static SRAM; DMA controller; on-chip OCP commutator (HUB); memory access arbiter; two RS-232 controllers (UART); three 64-bit interval timers; 2 x MIL-STD-1553B, ONFI, SPI, I²C and JTAG (IEEE 1149.1) controllers; input-output general-purpose controller GPIO (16 I/O LVTTTL lines); interrupt controller. Functional diagram of 1907VM038 chip is presented at Fig. 1.

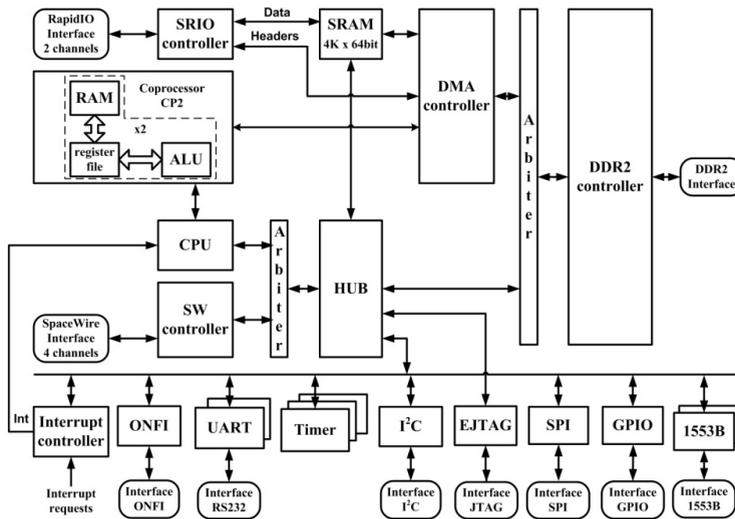


Fig. 1. Functional diagram of 1907VM038 microprocessor.

3.2. Multiport SpaceWire switch 1907VM056

System-on-chip (SOC) 1907VM056 is a 32-bit microprocessor with embedded MIL-STD-1553B and SpaceWire interface controllers. This chip is based on 0.25 mkm silicon-on-insulator (SOI) technology. System-on-chip 1907VM056 consists of: 32-bit RISC core processor compatible with KOMDIV architecture; universal data storage controller (including static RAM, ROM and PIO controllers); OCP internal bus controller; high-performance (up to 400 Mbit/sec) eight-channel SpaceWire controller (SW); two RS-232 controllers (UART); three 64-bit interval timers; I²C, two SPI, two MIL-STD-1553B and JTAG controllers; input-output general-purpose controller GPIO (32 I/O LVTTTL lines); interrupt controller. Functional diagram of 1907VM056 chip is presented at Fig. 2.

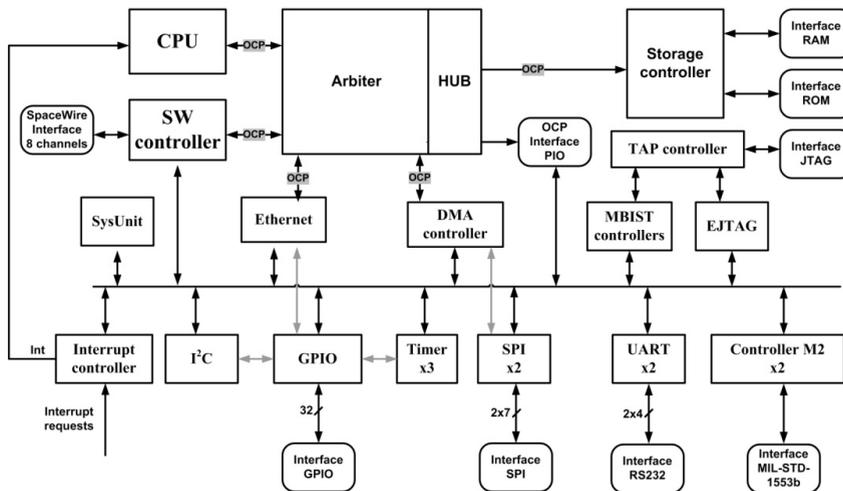


Fig. 2. Functional diagram of 1907VM056 multiport switch.

3.3. Multiport Serial RapidIO switch 1907KX018

Multiport 1907KX018 switch is intended for interconnection organization between systems with Serial RapidIO channels. This chip is based on 0.25 mkm silicon-on-insulator (SOI) technology. The 1907KX018 switch consists of: six 1x or 4x Serial RapidIO ports; switching unit with routing table; performance monitoring unit; registers unit; I²C and JTAG (IEEE 1149.1) controllers. Main distinctive features of 1907KX018 include separating routing table for each port, performance-monitoring system and embedded error correction unit. The switch is capable to interconnect up to 256 devices. Individual routing tables, loading either through Serial RapidIO ports or by I²C interface, allow flexible tuning of network packets transmission paths. Performance monitoring system is used to determine dataflow characteristics in channels and early diagnostic of network congestions. It allows reducing reserved channels reconnection time. Functional diagram of 1907KX018 chip is presented at Fig. 3.

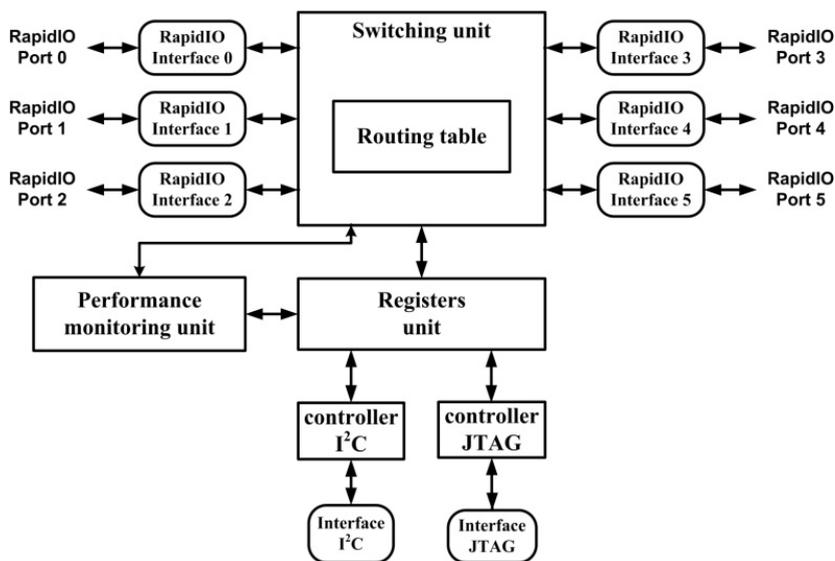


Fig. 3. Functional diagram of 1907KX018 multiport switch.

4. Scientific data acquisition system of GAMMA-400 scientific complex

Space project GAMMA-400 [7-8] is intended for investigation of cosmic gamma-emission in the energy band from ~20 MeV up to several TeV, electrons/positrons fluxes from ~1 GeV up to ~10 TeV and cosmic-ray nuclei fluxes with energies up to ~10¹⁵ eV by means of GAMMA-400 gamma-telescope [9-11] represents the core of the scientific complex (SC). The study of gamma ray bursts over virtually the entire celestial sphere in the energy band of 10 keV–15 MeV are possible too by means of KONUS-FG apparatus included in scientific complex.

The scientific data acquisition system (SDAS) developing by SRISA RAS is the information kernel of scientific complex. All mentioned above unification solutions were implemented during SDAS design stage. Fig. 4 shows the structure of the integrate control complex, which is a distributed system for acquisition, preprocessing, and registration data from scientific measuring systems (SMS) together with additional control means involving measuring systems and service systems of scientific complex. Data encryption is used to reduce the quantity of transmission failures. In order to increase the reliability, SDAS is made using a scheme with two hot- and cold-reserve subsystems. All SC-SDAS data exchange signals are double redundant; each redundant line is assigned with its own allocated data transceiver. Additional reliability level of SDAS is achieved by minimization of high integrity chips amount.

Precise timing of scientific data is maintained in SDAS by using signals from onboard time and frequency standard system (OTFS), forming a 32-bit serial onboard time code (OTC) transmitted to each SMS via GPIO/LVDS interface of central processing unit (CPU) of SDAS along with high-stable reference signals (SYNC).

The scientific data acquisition system carries out the following main functions:

- the data acquisition from measuring systems of scientific complex (up to 100 GByte per day);
- preliminary data processing of scientific information and storage it in nonvolatile mass memory (1 TByte total);
- scientific information transfer into high-speed (320 Mbit/sec) scientific radio line (SRL) for its transmission to data-acquisition ground stations;
- control information reception from spacecraft onboard control system (OCS), its decoding and transfer into SMS;
- receiving signals from OTFS/OCS and generating OTC and SYNC signals for SMS.

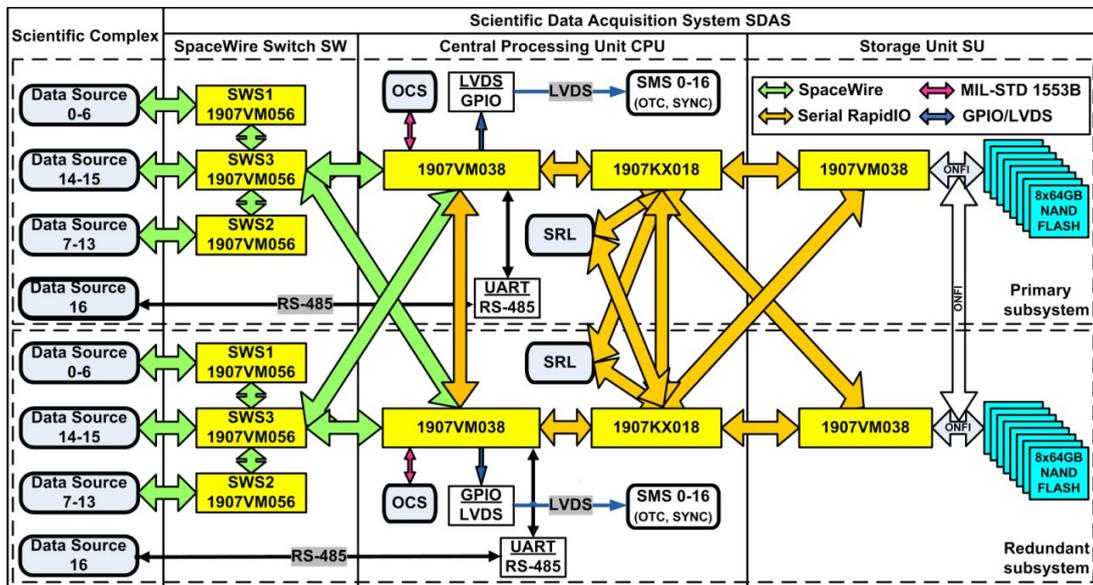


Fig. 4. Functional diagram of GAMMA-400 project scientific data acquisition system (OCS - onboard control system, SMS – scientific measuring system, SRL – high-speed scientific radio line, OTC – 32-bit onboard time code, SYNC – high-stable synchronization signals).

Data acquisition from SMS is divided into two dataflows. High-rate data sources 0-15 (see Fig. 4) is implemented by means of 16 high-speed SpaceWire channels with total throughput of ~70 MByte/sec. Data source 16 is intended for data acquisition from low-informative (~100 kByte/sec) KONUS-FG device via RS485 interface.

High-rate scientific information is transferred through twenty-channel SpaceWire switch based on three 1907VM056 chips (SWS unit, see Fig. 5) into central processing unit consisting of controlling microprocessor (1907VM038) and six-channel Serial RapidIO switch (1907KX018). CPU provides as the storage of preliminary processing scientific information into storage unit (SU) as the extracting of previously storage information from SU for its transmission to the data-acquisition ground stations through SRL simultaneously. The storage unit (see Fig. 6) consists of NAND flash array with total capacity of 1 TByte and operating microprocessor (1907VM038). Last one contains the full set of functional blocks quite enough for the management of NAND flash array of such capacity. The central processing unit (see Fig. 7) implements following set of functions:

- the receiving and checking of information from all data sources;
- preliminary data processing, information quotes control and data transmission through Serial RapidIO channels either into storage unit or scientific radio line;
- program commands receiving from onboard control system through multiplexed data channel (MIL-STD-1553B)

- and their translation into measuring systems of scientific complex through SpaceWire channels;
- receiving the signals from onboard time and frequency standard system and form 32-bit onboard time code and the set of synchronization signals transmitted to each scientific measuring system;
- pulse commands receiving from onboard control system and scientific telemetry information transmission into onboard telemetry system (OTS);
- periodically self-testing procedure;
- redundancy control, including the reserved transmission paths commutation for SpaceWire and Serial RapidIO networks.

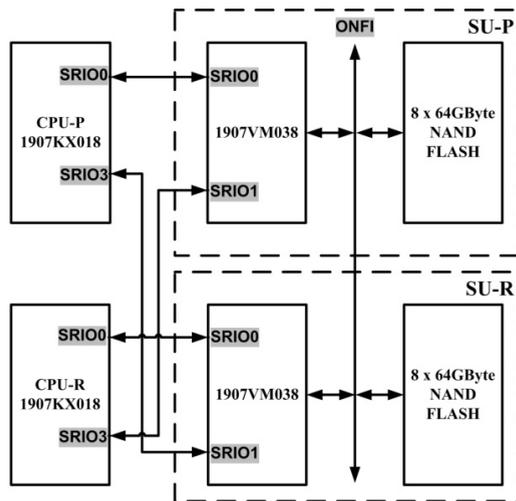
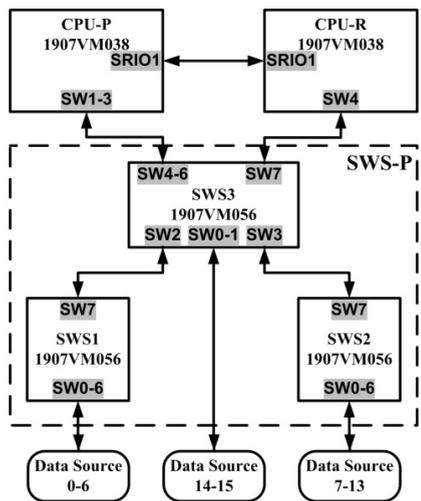


Fig. 5. Functional diagram of SpaceWare switch unit. Indexes P and R correspond to primary and redundant SDAS subsystems. SW0-SW7 – SpaceWare channels of 1907VM056 chip.

Fig. 6. Functional diagram of the storage unit. SRIO0-SRIO5 – Serial RapidIO channels of 1907KX018 and 1907VM038 chips.

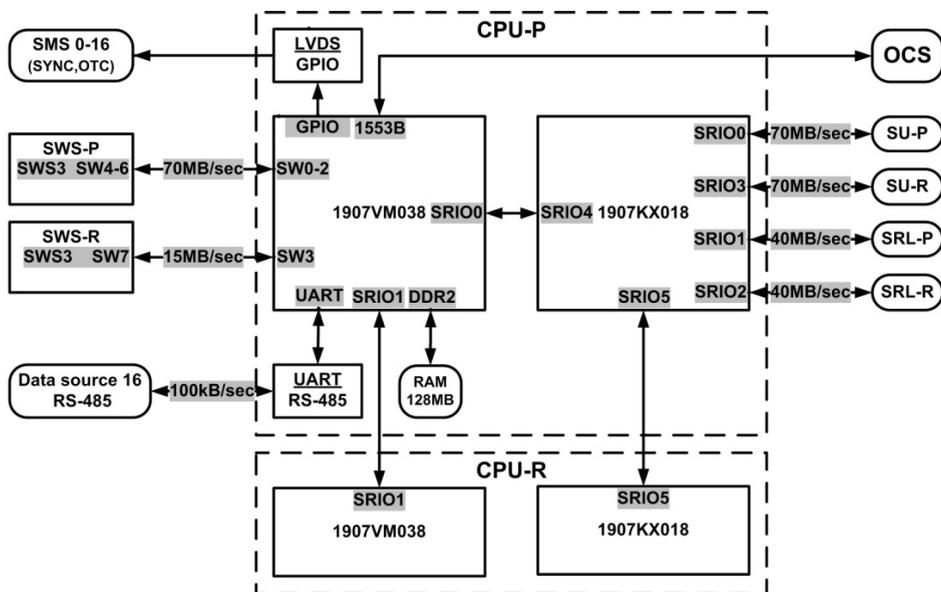


Fig. 7. Functional diagram of CPU unit. Indexes P and R correspond to primary and redundant SDAS subsystems.

As was mentioned above, SpaceWire network and Serial RapidIO network are based on twenty-channel SpaceWire switch (consisting three 1907VM056 chips) and 1907KX018 six-channel switch correspondingly. The last one is capable to switch simultaneous data flows in the non-blocking mode. For example, the data recording into storage unit and data reading from it and subsequent sending them into scientific radio line. The number of switch ports is enough for reconnecting of storage units and scientific radio line reserved blocks.

5. Conclusions

The problem of electronic component unification at different levels (circuits, interfaces, hardware and software) used in space industry is very important in relation to reducing of cost and development time. The space-qualified chips unification for the kernel level, external interfaces and data acquisition systems is achieved. To reduce power consumption and enhance data reliability, embedded system interconnect is made hierarchical: upper level is Serial RapidIO 1x or 4x with rate transfer of 1.25 Gbaud per line; next level - SpaceWire with rate transfer up to 400 Mbaud and lower level - MIL-STD-1553B and RS232/RS485. The Ethernet 10/100 is a technology interface and provided connection with the previously released modules.

On hardware level, implementation of two standard types: VPX (EUROMECHANICS standard, 6U form factor) for high-level performance systems and PCI/104-Express for compact systems is suggested.

As operating system, real-time OS Baget 3.0 made in compliance with international standards was chosen. This RTOS is flexible scheduling, easy portable on different computational platforms and has established a reputation in designing embedded control systems.

The described environment allows creating various architecture redundancy systems. Designers can develop heterogeneous systems that employ the highest peer-to-peer networking performance of Serial RapidIO while at the same time using multiprocessor clusters that may be either SpaceWire or Serial RapidIO connected.

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