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Abstract. The description of scientific data acquisition system (SDAS) designed by SRISA for the GAMMA-400 space project is presented. We consider the problem of different level electronics unification: the set of reliable fault-tolerant integrated circuits fabricated on Silicon-on-Insulator 0.25 mkm CMOS technology and the high-speed interfaces and reliable modules used in the space instruments. The characteristics of reliable fault-tolerant very large scale integration (VLSI) technology designed by SRISA for the developing of computation systems for space applications are considered. The scalable net structure of SDAS based on Serial RapidIO interface including real-time operating system BAGET is described too.

1. Introduction

The GAMMA-400 space project [1-5] is intended for investigation of cosmic γ-emission in the energy band from ~20 MeV up to several TeV, electron/positron fluxes from ~1 GeV up to ~10 TeV and cosmic-ray nuclei fluxes with energies up to ~10^{15} eV by means of GAMMA-400 gamma-telescope representing the core of the scientific complex. The investigation of gamma-ray bursts in the energy band of 10 keV–15 MeV are possible too by means of KONUS-FG apparatus included in the complex.

The scientific data acquisition system (SDAS) represents the information kernel of scientific complex and must be a high-reliable element. The SDAS is a distributed system for acquisition, pre-processing and registration data from scientific measuring systems (SMS) of scientific complex. Data encryption is used to reduce the quantity of transmission failures. In order to increase the reliability, SDAS is made using a scheme with two hot- and cold-reserved subsystems. All SMS-SDAS data exchange signals are double redundant. Each redundant line assigns with its own allocated data transceiver. Additional reliability level of SDAS is achieved by minimization of high integrity chips amount.

2. The scientific data acquisition system of the GAMMA-400 project

The main functions of the scientific data acquisition system (SDAS) are following:

- the data acquisition from SMS of scientific complex (up to 100 GByte per day);
- preliminary data processing of scientific information and storage it in nonvolatile mass memory (1 TByte total);

- scientific information transfer into high-speed (320 Mbit/sec) scientific radio line for its transmission to the data-acquisition ground stations;
- control information reception from spacecraft onboard control system via MIL-STD-1553B interface, its decoding and transfer into SMS;
- receiving signals from onboard time and frequency standard system and onboard control system and generating high-stable reference synchronization signals (1 Hz, 1 kHz and 1 MHz) and 32-bit onboard time code for precise timing of scientific data and transmitting them to each SMS via LVDS interface.

The functional diagram of SDAS is shown in figure 1. The SDAS consists of three types of modules: BTSSNI-201 (the central block with processing unit), BTSSNI-301 (data storage unit) and the control module BTSSNI-001. The main purpose of BTSSNI-001 is the conversion of the primary supply channel obtained from the power management system and the control of the supply channels for the modules. The primary and redundant modules with the control module BTSSNI-001 are set to the unifying board that is placed into the package. Processor elements are joined to the net using high-speed and high-reliable 1x 4x 1.25 Gbit/sec Serial RapidIO interface.

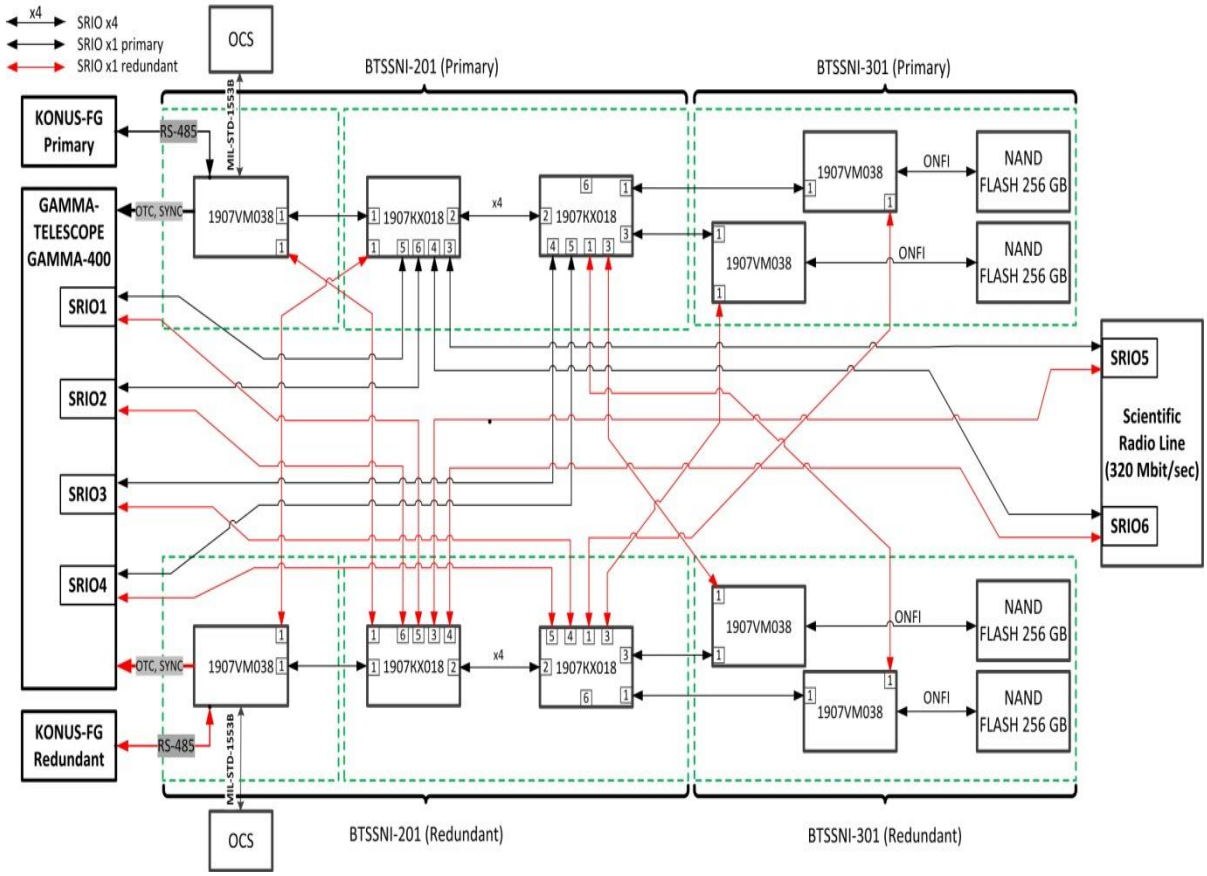

Figure 1. Functional diagram of GAMMA-400 project scientific data acquisition system (OCS - onboard control system, OTC – 32-bit onboard time code, SYNC – high-stable synchronization signals (1 Hz, 1 kHz, 1 MHz) , SRIO - Serial RapidIO interface, digits in squares are the identifiers of SRIO ports).

Data acquisition from SMS is divided into two data flows. The data acquisition from the gamma-telescope of scientific complex and scientific telemetry system is provided using four high-speed data acquisition Serial RapidIO channels with total throughput of ~70 MByte/sec. The scientific data is

transferred to the processing block, which consists of 1907VM038 device. This microprocessor provides both processed data storage and the fetch of data from the storage using six-port Serial RapidIO switch 1907KX018 to transfer it to the high-speed scientific radio line. The data acquisition from low-informative ~100 kbit/sec KONUS-FG device is realized via RS-485 interface. The data storage unit is designed using the system-in-package NAND flash memory. For the reliable transferring during the whole scientific complex lifetime (7-10 years), we use the redundant 1 TByte data storage.

The connection of SDAS with the onboard control system is provided using the redundant multiplexed channel MIL-STD-1553B and one-time pulse commands. The diagnostics of different SDAS nodes and control of temperature of "heating" VLSI are provided by onboard telemetry system.

Table 1 presents the distinctive features of radiation-tolerant VLSI designed by SRISA implemented in the SDAS.

Table 1. The distinctive features of VLSI implemented in SDAS of GAMMA-400 project [6].

Parameter	**1907VM038**	**1907KX018**
Clock rate	100 MHz	100 MHz
Serial RapidIO performance	1 channel 1x 4x 1.25 Gbit/sec	6 channels 1x 4x 1.25 Gbit/sec
SpaceWire performance	4 channels 400 Mbit/sec	-
SEL	none	none
SEE LET_{th} (without error correction)	~6 MeV·cm^2/mg	~6 MeV·cm^2/mg
σ_{sat}	< 3·10^{-8}cm^2/bit	< 3·10^{-8}cm^2/bit
TID_{Si}	≥ 50 krad	≥ 50 krad
Operating temperature	-60 ÷ +125°C	-60 ÷ +125°C
Power consumption	≤ 8 W	≤ 6 W
Package	DBGA 675	DBGA 399

System-on-chip 1907VM038 based on processor core KOMDIV-32 [7-10] is used for various onboard systems. It consists of 32-bit central processing unit (CPU), 128-bit arithmetic co-processor CP2, system controller with DDRII, SPI, 1.25 Gbit/sec Serial RapidIO, SpaceWire (4 channels), I^2C, GPIO, UART. Clock frequency is 100 MHz, the throughput of RAM is 512 MByte/sec.

The Serial RapidIO switch VLSI 1907KX018 is used for the connection of various switches and systems-on-chip. It consists of six Serial RapidIO ports; the transferring environment is configured independently: LP-Serial 4X or 1X. Maximum transferring speed is 1.25 Gbit/sec (per channel). It has the commutation table for each port, performance control system and built-in error-correcting block. The switch can directly connect up to 256 devices in the system, which is usually enough for the onboard systems. Individual commutation tables allow to flexibly configuring the transferring of data packages. The performance control system is used for the defining of characteristics of data flow in channel, overload detection, the localization of locking. The defining of the data flow is provided at the stage of net topology setting simulation and experimentally. The possible reasons of overloads can be the degradation of channels due to faults. Early detection of faults decreases the time needed to enable the reserved path. It is very useful that the switch can define the locked channels for the reserved path choosing. Maximum power consumption when all six ports in 4X mode are used is less than 6 W. In 1X mode or using the individual switching-off of an individual port's transmitter, the power consumption is reduced. The supply voltages are 2.5 V and 3.3 V. The high fault-tolerance is achieved using the error-correcting codes for the data package memory, the redundant commutation tables, the layout and circuit techniques at the standard cells level. The switch has the extended ability of the performance diagnostics. The state of diagnostics registers is available through I^2C interface, Also, the separate fault signals can be sent to the discrete signal port for the further analysis by the repairing system.

As operating system, real-time OS (RTOS) Baget 3.0 [11, 12] was chosen. This RTOS is developed based on the following general approaches:

- use of standards (ARINC 653 and POSIX 1003.1 for programming interface; C standard for C language and libraries);
- portability;
- advanced facilities for tracing, logging, diagnostics. and error handling (health monitor):
- flexible scheduling;
- object-oriented approach:
- scalability (configuration tools);
- instrumental software for developing and debugging user cross-applications;
- large number of environmental packages for creating graphics applications, databases, and mapping systems.

For the best portability, OS is divided on three main parts: main part independent on hardware, written on C language (the biggest); the second part, dependent only on central processor type, written on C or Assembler language (much smaller); modules support part containing modules drivers.

During software design, cross-development technology is used whereby, using the host computer with a general-purpose OS, the source codes and OS libraries are stored as well as the compilation and build of the boot image that is executed on the target computer under the control of RTOS are performed. For debugging in terms of the source code, a remote debugger is used.

3. Conclusion

The unification of space-grade chips is achieved at the core level, interfaces and the data transferring systems. The system is made hierarchical to reduce the power consumption and to increase the reliability. The upper level is switchable Serial RapidIO environment with 1.25 GByte/sec per channel. The lower level is low-speed multiplexed MIL-STD-1553B and RS-485 channels. The computation system hardware level is designed based on VPX standard.

During the current stage of GAMMA-project development, the prototype of SDAS was created. Experimental working-off of the main construction units in laboratory conditions has justified the engineering solutions and electronic elemental base selection for its design. The overall performance (>320 Mbit/sec) and power consumption (<80 W) of the SDAS satisfies all scientific complex requirements.

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